Result

The output of Logic Analyzer is shown below:

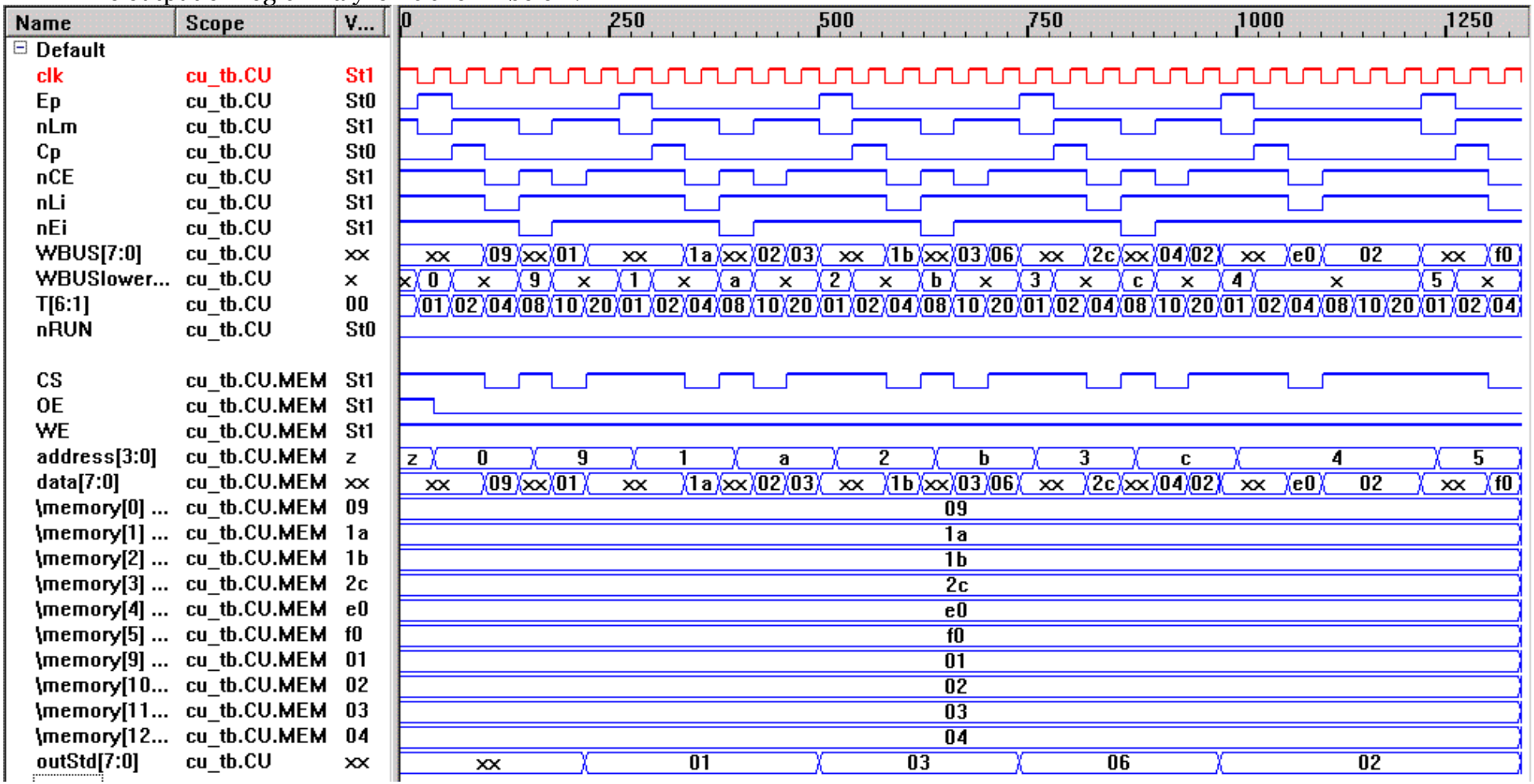

Illustration 1: Logic Analyzer trace for following instruction

```
memory[0] = 8'h09;      // LDA 9H
memory[1] = 8'h1A;      // ADD AH
memory[2] = 8'h1B;      // ADD BH
memory[3] = 8'h2C;      // SUB CH
memory[4] = 8'hE0;      // OUT
memory[5] = 8'hF0;      // HLT
memory[9] = 8'h01;
memory[10] = 8'h02;
memory[11] = 8'h03;
memory[12] = 8'h04;
```